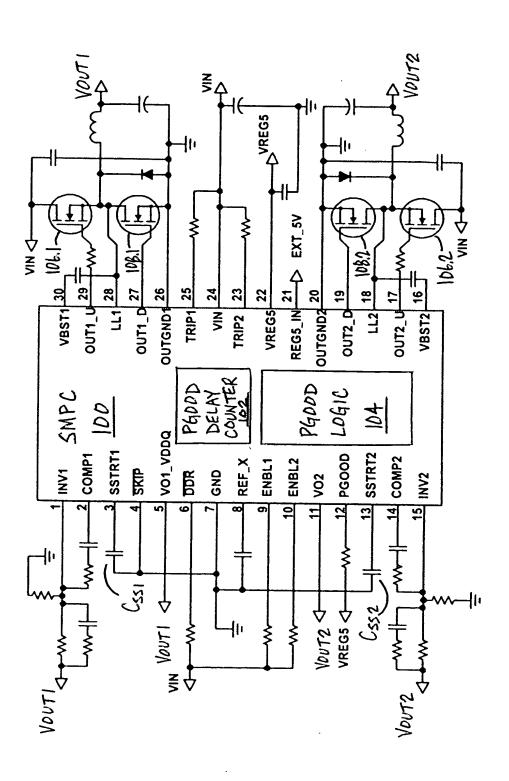
Inventor Name: Chaun Ni et al.
Docket No.: TI-36484 (UNITI-176XX)

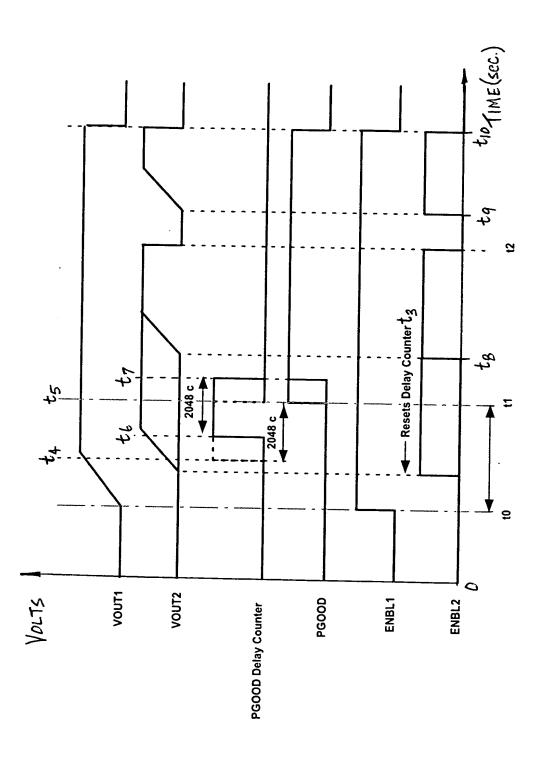
1/3



Fia. 1

Inventor Name: Chaun Ni et al.
Docket No.: TI-36484 (UNITI-176XX)





Title: ADVANCED MONITORING ALGORITHM FOR REGULATED POWER SYSTEMS WITH SINGLE OUTPUT FLAG

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Docket No.: TI-36484 (UNITI-176XX)

3/3

The PGOOD and ENBLx signals initially have low logical levels.

302

In the event an ENBLx signal is asserted high, the corresponding VOUTx signal (the "first output voltage") begins its soft-start.

304

In the event the first output voltage level comes within regulation and the soft-start voltage exceeds a predetermined threshold, the delay counter counts a total of 2048 clock cycles, at which time the first output voltage is considered stable and the PGOOD signal is asserted high.

306

In the event the another ENBLx signal is asserted high between the time the ENBLx signal is asserted high in step 304 and the time the first output voltage level comes within regulation in step 306, the corresponding VOUTx signal (the "second output voltage") begins its soft-start.

308

In the event the second output voltage level comes within regulation and the softstart voltage exceeds a predetermined threshold, the delay counter re-starts its counting of 2048 clock cycles, after which the first and second output voltages are considered stable and the PGOOD signal is asserted high.

310

In the event the other ENBLx signal is asserted high after the first output voltage level comes within regulation in step 306, that ENBLx signal is ignored until after the second output voltage finishes its soft-start.

312

In the event either the first or second output voltage falls out of regulation, or an under-voltage or other fault condition is detected while at least one respective ENBLx signal is high, the PGOOD signal is asserted low.

<u>314</u>

In the event the ENBLx signal corresponding to the first or second output voltage is asserted low while the other ENBLx signal remains high, the PGOOD signal maintains its high logical level and the disabled channel is ignored.

316